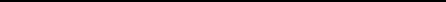


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<p>Sheet</p>		<p>1</p>	<p>of</p>	<p>2</p>	<p>Application Number .</p>
					<p>Filing Date</p>
					<p>First Named Inventor</p>
					<p>Andrews</p>
					<p>Group Art Unit</p>
					<p>Examiner Name</p>
					<p>Attorney Docket Number</p>
					<p>MS1-1378US</p>

Examiner Signature		Date Considered	4/1-05
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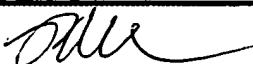
<sup>1</sup> Unique citation designation number. <sup>2</sup> See attached *Kinds of U.S. Patent Documents*. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

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				First Named Inventor	Andrews
				Group Art Unit	
				Examiner Name	
				Attorney Docket Number	MS1-1378US

<b>NON PATENT LITERATURE DOCUMENTS</b>					
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			T <sup>2</sup>
PWC		YAMACHI, et al.; "The Technique for Object and Collision Detection by Z-buffer"; Department of Computer and Information Engineering; Nippon Institute of Technology; Vol. 43; No. 6; June 2002; pp. 1899-1911. <i>Abstract only</i>			
/		WHITE, et al; "The Tayra 3-D Graphics Raster Processor; Comput. & Graphics, Vol. 21; No. 2; pp. 129-142; 1997			
/		BRESENHAM; "Teaching the graphics processing pipeline: cosmetic and geometric attribute implications"; Computers & Graphics 25 (2001) 343-349; 7pages.			
/		DOCTOR, et al; "Using raster scan in color graphics"; Mini-Micro Systems; December 1981; pp. 101-108			
/		WHITTED; "Hardware Enhanced 3-D Raster Display System"; CMCCS '81/ACCHO '81; pp. 349-356			
/		FUCHS et al; "Pixel-Planes: A VLSI-Oriented Design For 3-D Raster Graphics"; CMCCS '81/ACCHO'81; pp. 343-347			
/		PARKE; "Simulation and Expected Performance Analysis of Multiple Processor Z-Buffer Systems"; 1980 ACM 0-89791-021-4/80/0700-0048; pp. 48-56			
✓		CHEN et al.; "Reduce the Memory Bandwidth of 3D Graphics Hardware With a Novel Rasterizer"; Journal of Circuits, Systems, and Computers, Vol. 11; No. 4; (2002) pp. 377-391			
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		4-1-05

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